REMARKS

Claims 1-31 were rejected under 35 U.S.C. 102(b) as being anticipated by Chapman. Applicant respectfully traverses the rejections and requests reconsideration.

Claim 1 recites "storage means for holding packets of the input packet streams at addressable locations each identifiable by an address." The Examiner points to Chapman's input buffers as described at col. 2, lines 4-5. The buffers taught by Chapman perform traffic buffering. With reference to Figure 3, Chapman teaches input buffer 320/324. The input buffer 320/324 is a FIFO queue for temporary packet storage (see, col. 7, line 51). There is no teaching or suggestion in Chapman for these buffers 320/324 being addressable. More specifically, there is no teaching or suggestion that the FIFO queued data in the input buffer 320/324 stored packets "at addressable locations each identifiable by an address." Claim 1 accordingly is not anticipated by Chapman.

Claim 1 further recites "an assignment data structure identifying for each input stream at least one destination to which each input packet stream is to be routed." The Examiner points to Chapman's switch fabric as described at col. 3, line 34 and col. 6, lines 6-21. Applicants point out that the claim language recites a "data structure." The Examiner has identified apparatus in the form of a switch fabric, but fails to explain how this switch fabric would implement the claimed data structure. The switch fabric of Chapman, which is a ring communications network, is not in any way a "data structure" as claimed. Although the included nodes in the fabric have a memory (reference 810, Figure 8), there is no suggestion in Chapman that this memory stores data for "identifying for each input stream at least one destination to which each input packet stream is to be routed." Col. 12, lines 65-67 specifically mentions that the memory 810 does not include or store routing data. Claim 1 accordingly is not anticipated by Chapman.

Claim 1 still further recites "a packet allocation data structure holding for each new incoming packet a source identifier identifying the origin of the packet and the address in the storage means where the packet is held, the packet allocation data structure further holding information identifying the intended destination of the packet derived from the assignment data structure." The Examiner points to Chapman's routing table as described at col. 7, lines 65-67 and col. 10, lines 5-12. Applicants note that the routing table is not described by Chapman in any detail except that it maps destination addresses of incoming data packets to the switch output ports (col. 7, lines 65-67). In contrast, the claimed invention has "a packet allocation data structure" which holds "for each new incoming packet a source identifier[,] the address in the

storage means where the packet is held, [and] information identifying the intended destination of the packet." The routing table in Chapman identified by the Examiner does not hold information "for each new incoming packet." This is made clear by the fact that the mapping between destination addresses and output ports stored in the Chapman routing table is not modified when a new incoming data packet is received. Still further, the Chapman routing table does not store "a source identifier", the "address in the storage means where the packet is held", and "information identifying the intended destination of the packet" as claimed. The Examiner's analysis has wholly failed to address where and how the claimed information is being stored, and further has failed to identify "a packet allocation data structure" for holding this information. Chapman's focus on linking destination addresses and output ports does not contemplate storing data relating to a "source identifier" for each new incoming packet as claimed. The routing table data in Chapman further fails to include data identifying the "address in the storage means where the packet is held." Claim 1 accordingly is not anticipated by Chapman.

In view of the foregoing, Applicants respectfully submit that the Examiner has failed to show that the invention of claim 1 is anticipated by Chapman. Withdrawal of the Section 102 rejection is requested.

Claim 8 includes similar limitations as claim 1, and thus Applicants submit that claim 8 is not anticipated by Chapman for at least the same reasons as claim 1.

Turning next to claim 11, Applicants claim "holding each packet of the packet stream at an addressable location identifiable by an address in a storage means." The Examiner points to Chapman's input buffers as described at col. 2, lines 4-5. The buffers taught by Chapman perform traffic buffering. With reference to Figure 3, Chapman teaches input buffer 320/324. The input buffer 320/324 is a FIFO queue for temporary packet storage (see, col. 7, line 51). There is no teaching or suggestion in Chapman for these buffers 320/324 being addressable. More specifically, there is no teaching or suggestion that the FIFO queued data in the input buffer 320/324 be packets that are held (stored) "at an addressable location identifiable by an address." Claim 1 accordingly is not anticipated by Chapman.

Claim 11 further recites "holding for each new incoming packet a source identifier identifying the origin of the packet and the address in the storage means where the packet is held." The Examiner points to Chapman's routing table as described at col. 7, lines 65-67 and col. 10, lines 5-12. Applicants note that the routing table is not described by Chapman in any detail except that it maps destination addresses of incoming data packets to the switch output

ports (col. 7, lines 65-67). In contrast, the claimed invention holds "for each new incoming packet a source identifier[and] the address in the storage means where the packet is held." The routing table in Chapman identified by the Examiner does not hold information "for each new incoming packet." This is made clear by the fact that the mapping between destination addresses and output ports stored in the Chapman routing table is not modified when a new incoming data packet is received. Still further, the Chapman routing table does not store "a source identifier" and the "address in the storage means where the packet is held" as claimed. Chapman's focus on linking destination addresses and output ports does not contemplate storing data relating to a "source identifier" for each new incoming packet as claimed. The routing table data in Chapman further fails to include data identifying the "address in the storage means where the packet is held." Claim 11 accordingly is not anticipated by Chapman.

In view of the foregoing, Applicants respectfully submit that the Examiner has failed to show that the invention of claim 11 is anticipated by Chapman. Withdrawal of the Section 102 rejection is requested.

Claim 15 recites "a packet allocation table for associating a source and at least one destination for a particular packet with a memory location at which the particular packet is stored." The Examiner points to Chapman's routing table as described at col. 7, lines 65-67 and col. 10, lines 5-12. Applicants note that the routing table is not described by Chapman in any detail except that it maps destination addresses of incoming data packets to the switch output ports (col. 7, lines 65-67). In contrast, the claimed invention has "a packet allocation data structure" which associates "a source [and] destination for a particular packet with a memory location at which the particular packet is stored." The routing table in Chapman identified by the Examiner does not store "a source" identification, a "destination" identification and an association with a "memory location" where the packet is stored, as claimed. The Examiner's analysis has wholly failed to address where and how the claimed information is being stored, and further has failed to identify "a packet allocation table" for holding this information. Chapman's focus on linking destination addresses and output ports does not contemplate storing data relating to a "source" for a packet as claimed. The routing table data in Chapman further fails to include data identifying the "memory location" where the packet is stored. Claim 15 accordingly is not anticipated by Chapman.

Claim 18 is believed to be patentable over Chapman for at least the reasons recited above with respect to claim 15.

Claims 24 and 28 have been amended to clarify the claimed invention and further distinguish over the cited Chapman reference. There is no teaching or suggestion in Chapman for the claimed process for delivery in the instance of more than one identified destination wherein delivery/output of the packet is conditioned on each of the destinations being simultaneously available.

Applicant respectfully submits that all claims of the application are in condition for favorable action and allowance.

Dated: April 7, 2008

Respectfully submitted,

By /Andre M. Szuwalski/
Andre M. Szuwalski
Registration No.: 35,701
GARDERE WYNNE SEWELL LLP
3000 Thanksgiving Tower,
1601 Elm Street
Dallas, Texas 75201
(214) 999-4795
Attorney For Applicant